

New Tektronix Serial Analyzers Add to Comprehensive PCI Express 2.0 Test Solution

Provides Best Logic Analyzer Solution for PCIe 2.0; Provides Power Management and Cross Bus Analysis; New Probes Enable Easy Access

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Tektronix, Inc. , a leading worldwide provider of test, measurement and monitoring instrumentation, announced new TLA7S16 and TLA7S08 Serial Analyzers for test and validation of PCI Express (PCIe) 1.0 and 2.0 designs. Unlike competing protocol analyzers, the new Tektronix Serial Analyzer products uniquely provide detailed PCIe 2.0 protocol information along with cross-bus analysis. They augment the industry's most complete PCIe test solution, enabling the development of next-generation, high-speed computing platforms.

PCI Express 2.0 introduces performance enhancements for the computer, storage, and communications industries. The primary enhancement is the speed increase from 2.5 Gb/s to 5.0 Gb/s. The most significant validation challenges for PCIe 2.0 are capturing the signal at twice the speed, verifying power management, and performing cross-bus analysis. For power management, the number of lanes in use or "link width" (up to 16 lanes), speed of the link (from 2.5 Gb/s to 5.0 Gb/s), and idle states are dynamically negotiated to conserve power whenever possible. Power management is critical in systems whether it is implemented in a laptop to extend battery life or in a server system to conserve energy.

PCI Express 2.0

PCIe 2.0 is a three layered architecture with physical (electrical and logical sub-blocks), data link and transaction layers. The link width, initialization, and speed negotiation is performed within the logical sub-block of the physical layer. The data link layer is responsible for ensuring that data sent on the link is correct and is responsible to ensure that packets are reliably transmitted on the link. Finally, the transaction layer is responsible for constructing request/completion transactions, transaction layer packet flow control, and messaging.

"PCIe 2.0 brings a new set of validation challenges for design engineers," said Jit Lim, Director, Technology Solutions Group, Tektronix. "The ability to validate physical layer events is critical, coupled with the need to have complete system visibility to locate elusive problems that may have been propagated from other buses in the system. This requires test equipment that is capable of acquiring the PCIe signal through all of the dynamically changing states. The new Tektronix TLA7S08 and TLA7S16 Serial Analyzers are the best logic test solution for debug and validation of PCIe 1.0 and 2.0 designs."

In addition to the serial analyzers, new P6716/P6708 mid-bus probes and pre-release slot interposer probes are available to test and validate all layers of the PCIe 2.0 protocol. The new analyzers plug into Tektronix TLA7000 series logic analyzers adding the ability to debug and correlate general purpose signals and other system interconnects including memory and computer processors.

"The industry is beginning its delivery of PCI Express 2.0 rollout with the expected introduction of products and platforms later this year," said Jim Pappas, Director Technology Initiatives & Industry Marketing, Intel Corp. "Capable and comprehensive test tools to ensure proper operation and interoperability are an important factor to the continued success of PCI-Express 2.0, and Tektronix has played a key role in enabling PCI-Express 2.0 product delivery with its extensive suite of test solutions."

Power Management

PCI Express 2.0 link width and speed negotiation requires debugging the logical sub-block of the physical layer where logic analysis instruments are able to provide detailed data, unlike protocol analysis tools. The new Tektronix TLA7S08 and TLA7S16 Serial Analyzers can acquire x1, x4 links or x8 links respectively. Two TLA7S16 Serial Analyzers are used for bi-directional x16 links.

PCIe 2.0 links can change width (number of lanes) dynamically. For instance, an eight lane link (x8) could change to 4 lanes (x4) -- which requires less power -- and return back to x8 when this is needed by the system. The PCIe 2.0 specification also allows for the link to dynamically alternate the speed between 2.5 Gb/s to 5 Gb/s, supporting both PCIe 1.0 and 2.0 standards. Additionally, a link can go into idle power states during the short periods of time when it is not being utilized. It is critical to validate that these link operations are performed correctly during the width and speed changes and during transitions to and from power management states. The new Tektronix Serial Analyzers can uniquely validate and debug operation of these link processes.

Cross-Bus Analysis

As electronic systems become more complex, integration of parallel and high-speed serial buses in designs is increasingly common. In many cases, it is not possible to debug system level issues by looking only at the PCIe bus. An example would be a case where the PCIe link issues a memory read request to the processor. In turn, the processor issues a memory read request to DDR memory. If the DDR memory reads from the incorrect memory address, the incorrect data will be returned back to the PCIe link and will result in incorrect system behavior. The Tektronix TLA7000 logic analyzer is the only tool that is able to time correlate interactions between PCIe, processors, and memory using a single test platform.

PCI-Express 2.0 Probing

The TLA7S08 and TLA7S16 Serial Analyzers are complemented by a series of serial acquisition probes. Designers who have the flexibility to incorporate a mid-bus probe will benefit from the superior electrical performance of the P6708 half-width and P6716 full-width mid-bus probes. Narrower link widths can take advantage of the P6708 footprint that minimizes board real estate.

In many situations, probe accessibility is not considered at design time. Engineers are often faced with debugging their silicon on platforms that were designed by OEMs or ODMs and in many cases these platforms do not have probe access points. A slot interposer is an alternative probing method for devices that utilize the PCIe slot, such as graphics cards or host channel adapter cards. Pre-release slot interposers are available in x1, x4, x8, and x16 link widths.

Comprehensive Test Solution

The Tektronix TLA7000 Series Logic Analyzer, TLA7S16 and TLA7S08 Serial Analyzers, P6716/P6708 mid-bus probes and the pre-release slot interposer probes are used to test and validate all layers of the PCIe protocol: physical, data link, and transaction layers.

Below the logical sub-block of the physical layer is the electrical sub-block. Tektronix provides the most capable PCIe 2.0 test solution for the electrical sub-block comprised of industry leading DSA70000 real-time and DSA8200 sampling oscilloscopes, AWG7000 arbitrary waveform generators, and complete test software. This new generation of Tektronix measurement tools helps engineers with the test challenges presented by PCIe 2.0. These next-generation instruments and application software solutions are part of an entirely new and comprehensive test bench for high-speed serial data.

Pricing and Availability

Pricing for the new Serial Analyzers begins at \$55,000 U.S. MSRP. The units are available for order. Mid-bus probes begin at \$16,000 U.S. MSRP and are also available for order.

About Tektronix

Tektronix is a leading supplier of test, measurement, and monitoring products, solutions and services for the communications, computer, and semiconductor industries -- as well as military/aerospace, consumer electronics, education and a broad range of other industries worldwide. With 60 years of experience, Tektronix enables its customers to design, build, deploy, and manage next-generation global communications networks, advanced and pervasive technologies. Headquartered in Beaverton, Oregon, Tektronix has operations in 19 countries worldwide. Tektronix' Web address is <http://www.tektronix.com/>.

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