Tektronix Newsroom

Tektronix Launches New Toolset for Serial Data Link Analysis

Offers Integrated, Flexible, Easy-to-Operate Framework for In-Depth Analysis of High-Speed Serial and DDR Memory Buses

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BEAVERTON, Ore., Jan. 28, 2013 /PRNewswire/ -- Tektronix, Inc., the world's leading manufacturer of oscilloscopes, today announced a new Serial Data Link Analysis Visualizer software package (SDLA Visualizer) for Tektronix performance oscilloscopes including the DPO/DSA/MSO70000 Series. Designers working on next generation high-speed serial standards can use SDLA Visualizer to specify their link, de-embed any components from the measurement path, simulate virtual link components, apply equalization and take measurements at multiple points on the transmission line in a serial data system, module or chipset.

(Photo: http://photos.prnewswire.com/prnh/20130128/SF45838-INFO)
(Logo: http://photos.prnewswire.com/prnh/20130103/SF36616LOGO-b)

For designers doing physical layer characterization, debug, and compliance of computer, communications, and memory high speed buses, SDLA Visualizer enables them to confidently bridge the gap between modeling behavior and actual signal integrity performance. This in turn significantly reduces design cycle time and speeds up decision making on critical design projects.

"As serial data and memory standards become faster and more complex, designers require new more powerful and flexible tools to accurately characterize the signal under test," said Brian Reich, general manager, Performance Oscilloscopes Tektronix. "With SDLA Visualizer customers not only get sophisticated modeling capabilities to verify compliance to serial standards, they also achieve a seamless transition between characterization, compliance, and debug environments."

Starting with USB 3.0, the latest serial technologies require sophisticated link analysis software that considers all components of the network, measurement equipment, and silicon specific IP models. Similarly, embedded designers who need to implement faster links in systems face challenges with probing signals at the desired test point and must remove reflections and other effects in order to see the true signal.

To meet these needs, SDLA Visualizer provides complete 4-port modeling and takes into account transmitter output impedance, scope and receiver input impedance, and channel and fixture impedance to provide the truest representation of the signal possible. This is accomplished by accounting for reflections, insertion loss and cross coupling terms of each element in the link. It also enables the user to validate and debug S-parameters on individual link elements on demand, saving the user time and providing element by element or visibility at any test point in the link.

Another key challenge is validating the link model. SDLA makes this task easier with a complete set of plots including frequency response, phase response, and plots of all 16 S-parameters. Adding to its usability, SDLA provides a single common user interface to define all link components while giving the user the flexibility to define multiple test points instead of having to create a different link model for each test point. SDLA Visualizer coupled with DPOJET Jitter and Eye Analysis software allows the user to validate the eye and jitter results at multiple test points simultaneously, providing confidence that the model is configured correctly.

IBIS AMI Model Integration
To make it easier to work with silicon-specific IP models, the SDLA Visualizer goes beyond supporting reference receiver equalization techniques and can incorporate vendor-specific receiver equalization and clock recovery algorithms to help configure and define the link model. These are often based on the IBIS Algorithmic Modeling Interface (IBIS-AMI) modeling standard for serial physical layer (PHY) links.

"Systems designers are using IBIS-AMI models to design and validate high speed links prior to PCB fab-out, with model accuracy being a major concern." said Barry Katz, CEO, SiSoft, a leading provider of EDA simulation software for system-level high-speed design. "Customers need a straightforward method to correlate models to measurements and perform real-time what-if analysis on lab hardware. With its new SDLA framework, Tektronix sets the foundation for signal integrity lab capabilities where this level of integration will be common practice."

Availability
The new SDLA Visualizer software will be available for customer download by the end of Q1 2013 worldwide. Contact your Tektronix account manager for details.

Wondering what else Tektronix is up to? Check out the Tektronix Bandwidth Banter blog and stay up to date on the latest news from Tektronix on Twitter and Facebook.

About Tektronix
For more than sixty-five years, engineers have turned to Tektronix for test, measurement and monitoring solutions to solve design challenges, improve productivity and dramatically reduce time to market. Tektronix is a leading supplier of test equipment for engineers focused on electronic design, manufacturing, and advanced technology development. Headquartered in Beaverton, Oregon, Tektronix serves customers worldwide and offers award-winning service and support. Stay on the leading edge at www.tektronix.com.

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