

Tektronix to Showcase ASIC Prototyping Debug Solution at Design Automation Conference 2013

Attendees Will Experience Firsthand RTL Simulation-Level Visibility to Multi-FPGA Prototypes Eliminating Recompiles for Faster, More Efficient Debug

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BEAVERTON, Ore., May 13, 2013 /[PRNewswire](http://prnewswire.com)/ -- Tektronix, Inc., a leading worldwide provider of test, measurement and monitoring instrumentation, today announced it will showcase its recently introduced [Certus 2.0](#) ASIC prototyping debug solution at the 2013 Design Automation Conference in Austin, TX, June 2-6, Booth 819. DAC is the premier conference devoted to the design and automation of electronic systems (EDA), embedded systems and software (ESS), and intellectual property (IP).

(Logo: <http://photos.prnewswire.com/prnh/20130103/SF36616LOGO-b>)

Shown for the first time at the Design Automation Conference (DAC) the Certus 2.0 suite of software and RTL-based embedded instruments fundamentally changes the ASIC prototyping flow by enabling full RTL-level visibility and making FPGA internal visibility a feature of the prototyping platform. This simulation-level visibility allows engineers to diagnose multiple defects in a day versus a week or more with existing tools.

"Proactive debug capability for ASIC prototypes has been missing within the FPGA ecosystem," said Dave Farrell, general manager for the embedded instrumentation group at Tektronix. "DAC attendees will now be able to see firsthand how Certus 2.0 fundamentally changes the ASIC prototyping flow and dramatically increases debug productivity."

Proactive debug strategy

Certus 2.0 allows designers to automatically instrument all the signals likely to be needed in each of the FPGAs in a multi-FPGA ASIC prototype with a small FPGA LUT impact. This enables a proactive debug and instrumentation strategy, eliminating the need to re-compile the FPGA to debug each new behavior, typically a painful eight to eighteen hour ordeal with traditional tools. Other key capabilities include:

- Automatic identification and instrumentation of RTL signals based on type and instance name including flip-flops, state machines, interfaces and enumerated types
- On-chip, at-speed capture and compression of many seconds of data without special external hardware or consuming FPGA I/O resources
- Advanced on-chip triggering bringing the power of logic analyzer trigger methods to embedded instrumentation
- Time-correlated capture results across clock domains and multiple FPGAs providing a system-wide view of the entire target design

Certus 2.0 works on any existing commercial or custom ASIC prototyping platform, and does not need special connectors, cables, or external hardware.

Tektronix Embedded Instrumentation Solutions

Following the acquisition of Veridae Systems in 2011, [Tektronix Embedded Instrumentation](#) solutions reflect the growing importance of Electronic Design Automation (EDA) software in helping engineers solve difficult instrumentation and debug challenges.

Wondering what else Tektronix is up to? Check out the Tektronix [Bandwidth Banter blog](#) and stay up to date on the latest news from Tektronix on [Twitter](#) and [Facebook](#).

About Tektronix

For more than sixty-five years, engineers have turned to [Tektronix](#) for test, measurement and monitoring solutions to solve design challenges, improve productivity and dramatically reduce time to market. Tektronix is a leading supplier of [test equipment](#) for engineers focused on electronic design, manufacturing, and advanced technology development. Headquartered in Beaverton, Oregon, Tektronix serves customers worldwide and offers award-winning [service](#) and [support](#). Stay on the leading edge at www.tektronix.com.

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